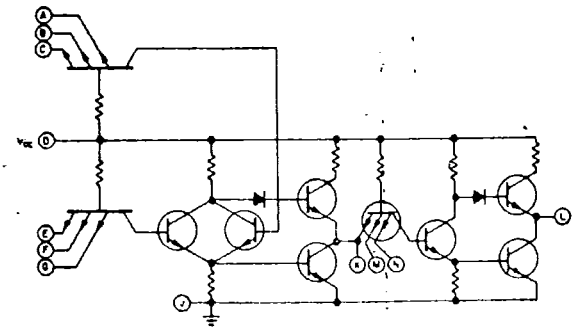
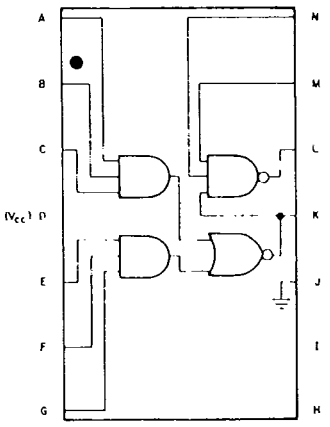
INTEGRATED CIRCUITS SUHL*

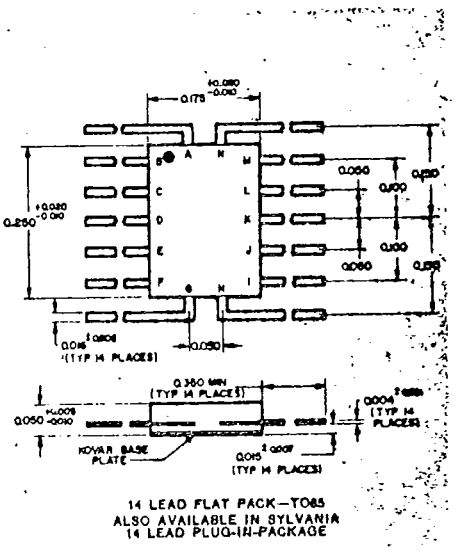
Exclusive-OR With Complement

SG90/SG91

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to +125°C







14 LEAD FLAT PACK—TO85
ALSO AVAILABLE IN SYLVANIA
14 LEAD PLUG-IN-PACKAGE

TRUTH TABLE

X	Y	K	Z	L
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1

where $X = A \cdot B \cdot C$
$Y = E \cdot F \cdot G$
$Z = K \cdot M \cdot N$

LOGIC EQUATIONS

(+) LOGIC

$K = \overline{(A \cdot B \cdot C) + (E \cdot F \cdot G)}$

$L = \overline{(K \cdot M \cdot N)}$

$L = A \cdot B \cdot C + E \cdot F \cdot G + \overline{M} + \overline{N}$

(−) LOGIC

$K = \overline{(A + B + C) \cdot (E + F + G)}$

$L = \overline{(K + M + N)}$

$L = (A + B + C) \cdot (E + F + G) \cdot \overline{M} \cdot \overline{N}$

CIRCUIT DESCRIPTION

The **SG 90** and **SG 91**, Exclusive-OR gates with Complement, are members of the SUHL* family of logic elements which is a monolithic, epitaxial, saturated high speed logic family. Each package contains two three-input AND gates which are OR'ed together and then inverted. This output, having full fan out, is available and is also fed into a NAND gate which provides the complement. Typical applications for this circuit are in full adders and parallel subtractors. The circuit is designed for high speed operation over the military temperature range of − 55 C to + 125 °C without sacrificing characteristics of fan out, logic swing, noise immunity and capacitance drive at low power.
This circuit requires a single power supply and has the following outstanding features:

CHARACTERISTIC SUMMARY

1. High fan out: 15 min for **SG 90**; 7 min for **SG 91**.
2. High speed: designed to operate at 20 mc, propagation delay time is typically 11 nsec per stage.
3. High noise immunity: ± 900 mV at 25°C and worst case fan out;
   + 450 mV from − 55°C to +125°C at worst case fan out;
   + 600 mV from 0° C to +75°C at worst case fan out.
4. High capacitance drive: up to 600 pf.
5. High logic swing: logic 0 is typically 0.26 volts;
   logic 1 is typically 3.3 volts at 25 °C.
6. Short circuit protection.
7. Low power: 35 mw average dissipation.
8. Low output impedance in the 0 and 1 level reduces noise pickup.
9. No complex loading rules since input and output are isolated.

These features offer to the logic designer for the first time in an integrated circuit the combined advantages of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital element that facilitates system design when combined with other SUHL elements.

* Sylvania Universal High level Logic

SG---00090-1X

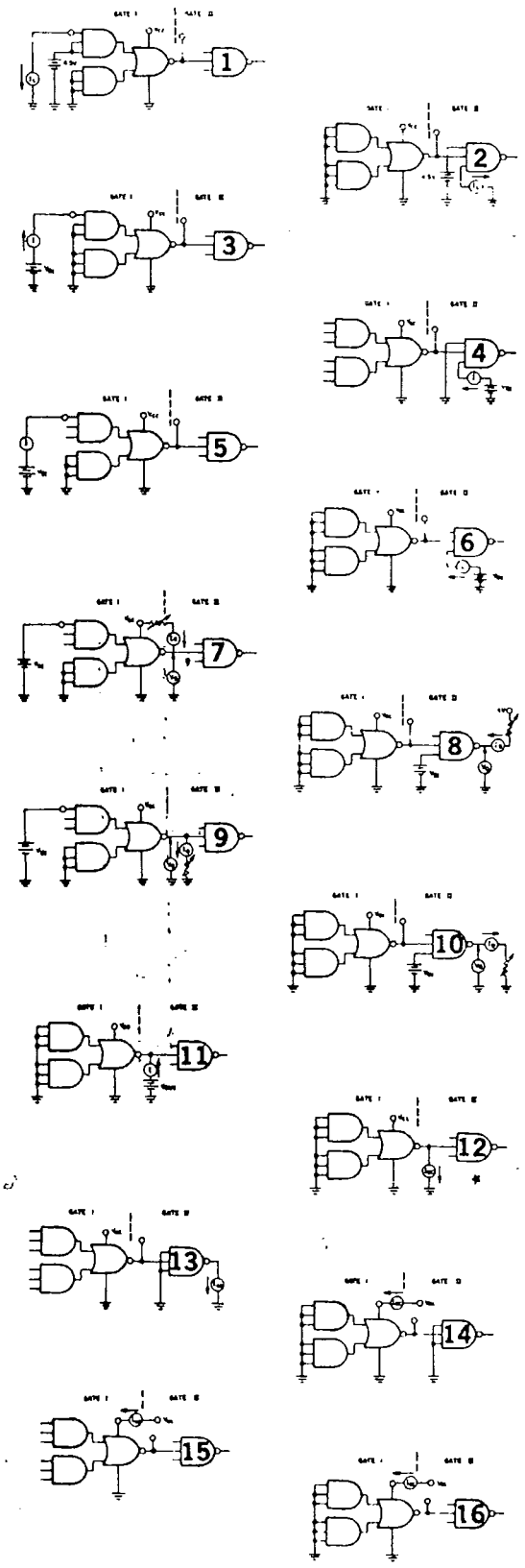
RATINGS

	Min.	Typical	Max.
VOLTAGE			
Supply voltage (D.C.)			8.0 V_{DC}
Supply voltage (surge, 1 sec)			12.0 V
Supply voltage (operating)	4.5	5.0	6.0 V
Input voltage			5.5 V
Output voltage			5.5 V

	Min.	Typical	Max.
TEMPERATURE AND POWER			
Operating	55		125 C
Storage	65		200 C
Thermal gradient, junction to air (θja)			0.3 C/MW
Thermal gradient, junction to case (θjc)			0.1 C/MW
Power Dissipation (50% Duty Cycle, V_{CC} = 5v)		35	MW

ELECTRICAL CHARACTERISTICS

Characteristics at V_{CC} = +5.0V	Symbol	Values at Required Temperatures −55°C	+25°C	+125°C	Units	Fig. No.
INPUT:						
Input Load Current (Gate I)	$I_{L(I)}$	1.33	1.33	1.33	mA Max.	
@ V_{in} =		0	0	0	Volts	1
Other Inputs @		4.5	4.5	4.5	Volts	
Input Load Current (Gate II)	$I_{L(II)}$	1.33	1.33	1.33	mA Max.	
@ V_{in} =		0	0	0	Volts	2
Other Inputs @		4.5	4.5	4.5	Volts	
Input Leakage Current (Gate I)	$I_{IN\ LK(I)}$	0.1	0.1	0.1	mA Max.	
@ V_{in} =		4.5	4.5	4.5	Volts	3
Other Inputs @		0	0	0	Volts	
Input Leakage Current (Gate II)	$I_{IN\ LK(II)}$	0.1	0.1	0.1	mA Max.	
@ V_{in} =		4.5	4.5	4.5	Volts	4
Other Inputs @		0	0	0	Volts	
Inverse Beta Current (Gate I)	$B_{INV(I)}$	0.1	0.1	0.1	mA Max.	
@ V_{in} =		4.5	4.5	4.5	Volts	5
Other Inputs @		Open	Open	Open		
Inverse Beta Current (Gate II)	$B_{INV(II)}$	0.1	0.1	0.1	mA Max.	
@ V_{in} =		4.5	4.5	4.5	Volts	6
Other Inputs @		Open	Open	Open		
Input (Off Level) Breakdown Voltage (Gate I)	$BV_{IN\ "I"(I)}$	5.5	5.5	5.5	Volts Min.	
@ I_{in} =		1.0	1.0	1.0	mA	3
Other Inputs @		0	0	0	Volts	
Input (Off Level) Breakdown Voltage (Gate II)	$BV_{IN\ "I"(II)}$	5.5	5.5	5.5	Volts Min.	
@ I_{in} =		1.0	1.0	1.0	mA	4
Other Inputs @		0	0	0	Volts	
Input (On Level) Breakdown Voltage (Gate I)	$BV_{IN\ "O"(I)}$	5.5	5.5	5.5	Volts Min.	
@ I_{in} =		1.0	1.0	1.0	mA	5
Other Inputs @		Open	Open	Open		
Input (On Level) Breakdown Voltage (Gate II)	$BV_{IN\ "O"(II)}$	5.5	5.5	5.5	Volts Min.	
@ I_{in} =		1.0	1.0	1.0	mA	6
Other Inputs @		Open	Open	Open		
Logic "I" Threshold Voltage (Gate I)	$V_{TH\ "I"(I)}$	2.0	1.7	1.4	Volts	
V_{out} =		0.45	0.45	0.45	Volts Max.	
I_{out} (SG90) =		20	20	20	mA	7
I_{out} (SG91) =		10	10	10	mA	
Logic "I" Threshold Voltage (Gate II)	$V_{TH\ "I"(II)}$	2.0	1.7	1.4	Volts	
V_{out} =		0.45	0.45	0.45	Volts Max.	
I_{out} (SG90) =		20	20	20	mA	8
I_{out} (SG91) =		10	10	10	mA	
Logic "O" Threshold Voltage (Gate I)	$V_{TH\ "O"(I)}$	1.0	1.2	0.9	Volts	
V_{out} =		2.5	2.4	2.7	Volts Min.	
I_{out} (SG90) =		1.5	1.5	1.5	mA	9
I_{out} (SG91) =		0.7	0.7	0.7	mA	
Logic "O" Threshold Voltage (Gate II)	$V_{TH\ "O"(II)}$	1.0	1.2	0.9	Volts	
V_{out} =		2.5	2.4	2.7	Volts Min.	
I_{out} (SG90) =		1.5	1.5	1.5	mA	10
I_{out} (SG91) =		0.7	0.7	0.7	mA	
OUTPUT:						
Output Leakage (I) & Beta Inverse (II)	$I_{O\ LKG}$	1.25	1.25	1.25	mA Max.	
V_{out} =		5.5	5.5	5.5	Volts	11
V_{in} =		0	0	0	Volts	
Output Short Circuit Current (Gate I)	$I_{SC(I)}$	10	10	10	mA Min.	
		45	45	45	mA Max.	12
Inputs @		0	0	0	Volts	
Output Short Circuit Current (Gate II)	$I_{SC(II)}$	10	10	10	mA Min.	
		45	45	45	mA Max.	13
Inputs @		0	0	0	Volts	
Logic "O" Level (Gate I & Gate II)	Logic "0"	0.40	0.40	0.45	Volts Max.	7 &
@ V_{in} =		2.8	2.8	2.8	Volts	
I_{out} (SG90) =		20	20	20	mA	8
I_{out} (SG91) =		10	10	10	mA	
Logic "I" Level (Gate I & Gate II)	Logic "1"	2.8	3.2	3.35	Volts Min.	9 &
@ V_{in} =		0.45	0.45	0.45	Volts	
I_{out} (SG90) =		1.5	1.5	1.5	mA	
I_{out} (SG91) =		0.7	0.7	0.7	mA	10
POWER REQUIREMENTS:						
Breakdown Voltage	BV	8	8	8	Volts Min.	
@ I_{cc} =		34	34	34	mA	14
Inputs @		0	0	0	Volts	
Current Drain — Gate I "ON" & II "OFF"	$I_{CC\ 1}$	10	10	10	mA Max.	
Inputs @		Open	Open	Open		15
Current Drain — Gate I "OFF" & II "ON"	$I_{CC\ 2}$	10	10	10	mA Max.	
Inputs Gate I @		0	0	0	Volts	16
Current Drain — Gates "OFF"	$I_{CC\ 3}$	7	7	7	mA Max.	
Inputs @		0	0	0	Volts	14

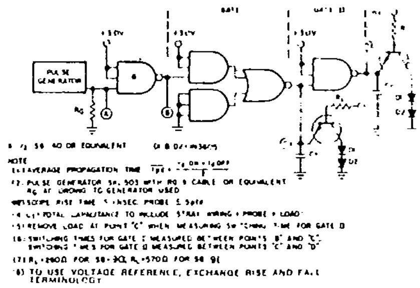


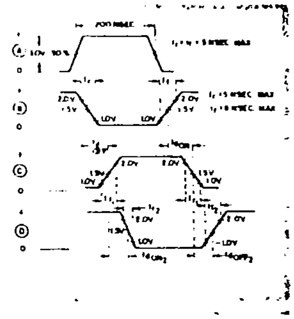
SG---00090-2X

*Short circuit only one output at a time

SWITCHING

SWITCHING CHARACTERISTICS	CONDITIONS: V_{CC} volts	T_A °C	FANOUT SG90	FANOUT SG91	C_T pfd.	LIMITS: TIME — nsec Min. GATE I	Max. GATE II
Turn On Delay	+5.0	+25	15	7	15	22	20
Turn Off Delay			15	7	15	22	20
Rise Time Note 8			15	7	15	6.0	5.0
Fall Time Note 8			15	7	15	8.0	8.0

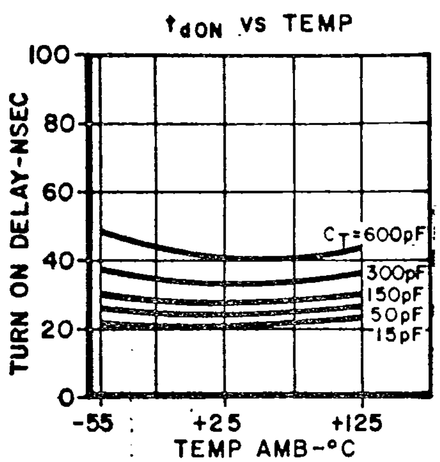


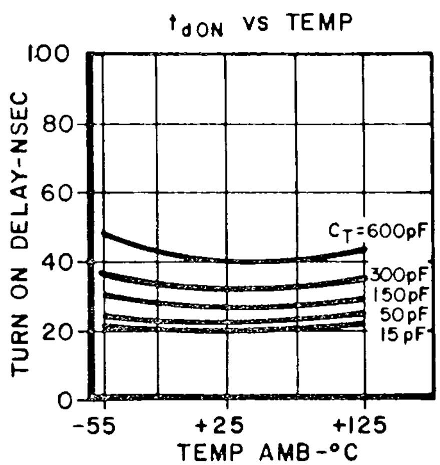


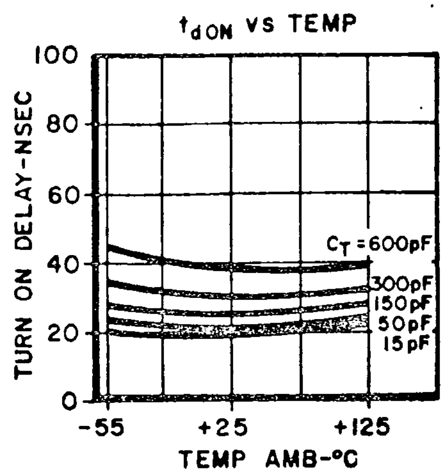
TYPICAL SWITCHING CHARACTERISTICS: V_{CC} = +5.0V

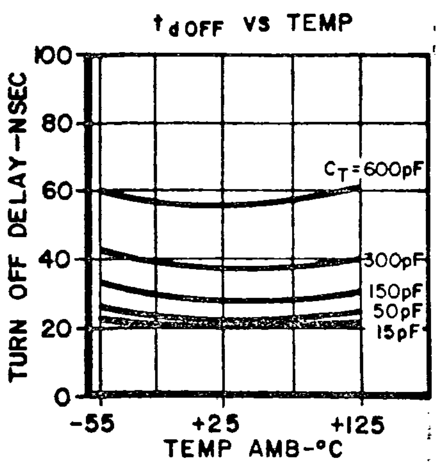
Shown below are typical characteristics for total propagation delay through Gate I, (the AND-NOR portion) and Gate II, (the following inverter). For typical switching characteristics of Gate I above refer to the SG110 series data sheet. For typical switching characteristics of Gate II above refer to the SG40 series data sheet.

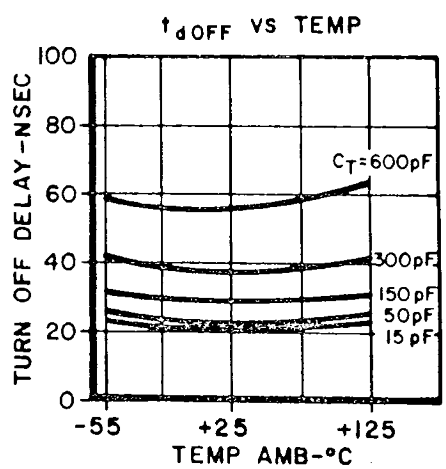
FAN OUT = 1 | **FAN OUT = 7** | **FAN OUT = 15**

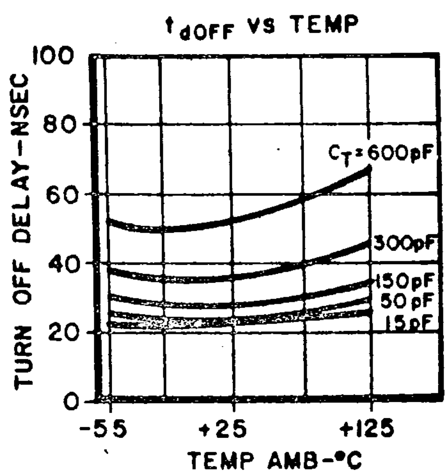












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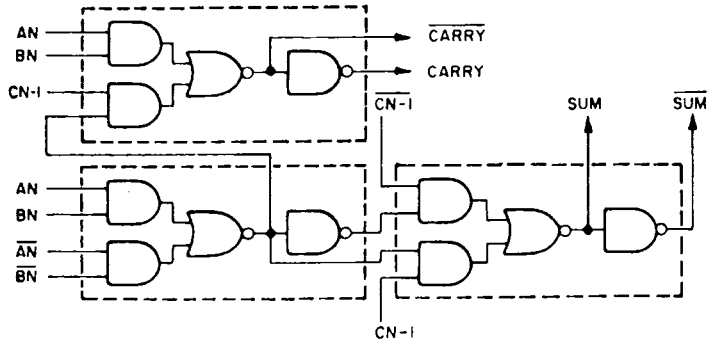
APPLICATION 1.
Full Adder

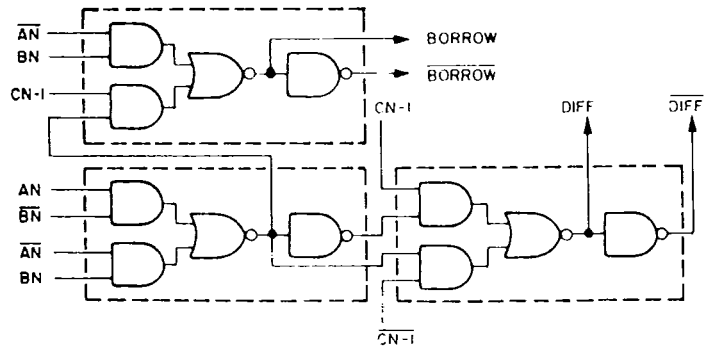


SUM = $\overline{AN}\ \overline{BN}\ CN\text{-}1 + \overline{AN}\ BN\ \overline{CN\text{-}1} + AN\ \overline{BN}\ \overline{CN\text{-}1} + AN\ BN\ CN\text{-}1$
CARRY = $AN\ BN + AN\ CN\text{-}1 + BN\ CN\text{-}1$

TRUTH TABLE

AN	BN	CN-1	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

APPLICATION 2.
Parallel Subtractor

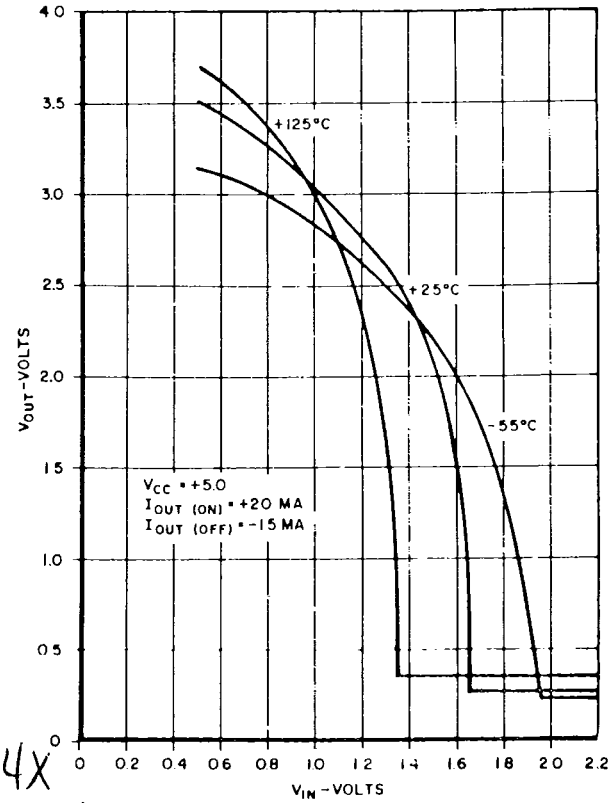


DIFF = $\overline{AN}\ \overline{BN}\ CN\text{-}1 + \overline{AN}\ BN\ \overline{CN\text{-}1} + AN\ \overline{BN}\ \overline{CN\text{-}1} + AN\ BN\ CN\text{-}1$
BORROW = $\overline{AN}\ BN + \overline{AN}\ CN\text{-}1 + BN\ CN\text{-}1$

TRUTH TABLE

AN	BN	CN-1	DIFF	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

TYPICAL V_{IN}-V_{OUT} TRANSFER CHARACTERISTIC
-55 C TO +125 C



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